REMARKS

Claims 3, 5-11, 14, 16-22, 25, and 27-33 are pending in the application. The Examiner's reconsideration of the rejections in view of the amendments and remarks is respectfully requested.

Claims 25, 27-29, and 31-33 have been rejected under 35 USC 101, as being directed to non-statutory subject matter. The Examiner stated essentially that there is no clear result - that the application of storage of the address is not clear.

Referring to Claims 25 and 27, the limitation "updating at least one of the words..." is believed to be a clear result. For example, the claimed invention performs an update of a word as part of a logical operation - such an update is a function of the claimed machine performing method steps embodied in the claimed program storage device.

Referring to Claims 31 and 32: the limitation "accessing the vector data file for the data vector..." is believed to be a clear result. For example, the claimed invention performs an access of the vector data file for the data vector as a function of the claimed machine performing method steps embodied in the claimed program storage device.

Referring to Claim 33: Claim 33 claims, *inter alia*, "performing a read or a write operation that addresses a vector in the vector data file via an index into the pointer array specifying an entry having a plurality of addresses corresponding to different elements of a vector in the vector data file, wherein the read or write operation accesses the vector to execute an instruction of the program of instructions." Claim 33 is believed to perform a function for

producing a result - for example, an operation accesses the vector via a pointer array to execute an instruction of the program of instructions.

Claims 28 and 29 depend from Claim 27. The dependent claims are believed to be allowable for at least the reasons given for Claim 27.

Reconsideration of the rejection is respectfully requested.

Claims 3, 8, 9-11, 14, 19-22, 25 and 31-33 have been rejected under 35 USC 103(a) as being unpatentable over Fossum et al. (USPN 4,888,679) in view of Birrittella (USPN 6,266,759). The Examiner stated essentially that the combined teachings of Fossum and Birrittella teach or suggest all of the limitations of Claims 3, 8, 9-11, 14, 19-22, 25 and 31-33.

Claims 3, 9, 10, 11, 14, 25, and 31-33 are the independent claims.

Claims 3, 9, 10, and 11 recite, *inter alia*, "a pointer array electrically coupled by a bus to the vector data file, the pointer array including a plurality of entries wherein each entry identifies at least one storage element in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file, wherein the words are addressed by a word address decoder coupled to the pointer array." Claims 14, 25 and 31 claim, *inter alia*, "providing a pointer array having a plurality of entries, wherein each entry identifies at least one storage element in the vector data file for storing at least one data element of the data vectors, wherein for at least one particular entry in the pointer array, the at least one storage element identified by the particular entry has an arbitrary starting address in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file." Claim 32 claims, *inter alia*, "providing a pointer array having a plurality of entries, wherein each entry identifies at least one storage

element in the vector data file for storing at least one data element of the data vectors, wherein for at least one particular entry in the pointer array, the at least one storage element identified by the particular entry has an arbitrary starting address in the vector data file, wherein the entries having arbitrary starting addresses are grouped into addressable words corresponding to individual data vectors stored in the vector data file" (emphasis added). Claims 33 claims, *inter alia*, "providing a pointer array having a plurality of entries, wherein each entry identifies at least one storage element in the vector data file for storing at least one data element of the data vectors, wherein for each entry in the pointer array, the at least one storage element identified by the particular entry has an arbitrary starting address in the vector data file, wherein the entries are grouped into addressable words, each addressable word comprising the arbitrary starting addresses corresponding to the storage elements of an individual data vector stored in the vector data file; wherein, for any given entry in the pointer array, the at least one storage element identified by the any given entry is independent with respect to the at least one storage element identified by other entries of the pointer array" (emphasis added).

Fossum teaches a vector stored in main memory (see FIG. 3) addressed by an address register and adder (see col. 8, line 60 to col. 9, line 15). Fossum does not teach or suggest that "entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file" as claimed in Claims 3, 9, 10, 11, 14, 25, and 31-33. Consider first that the vector of Fossum is not a vector data file - the vector of Fossum is merely vector in main memory. Further, entries in a address register of Fossum are not grouped into addressable words. The address register of Fossum is used in calculating addresses of vector elements using an adder or length counter. The calculating of individual vector elements is not analogous to an

addressable word. Therefore, Fossum fails to teach all the limitations of Claims 3, 9, 10, 11, 14, 25, and 31-33.

Referring to the point 7 of the Office Action, wherein the Examiner stated essentially that "Fossum also taught entries grouped in addressable words by the address decoder corresponding to the vectors", Applicants respectfully disagree. Fossum teaches that a block includes a quad-word composed on eight contiguous bytes, also called a data element (see col. 7, lines 2-8). The claimed invention includes limitations directed to entries having arbitrary starting addresses, wherein the entries are grouped into addressable words. Fossum does not teach or suggest bytes of the quad-word having arbitrary starting addresses; the bytes of the quad-word of Fossum are contiguous requiring only a single address to address all of the bytes of the entire quad-word. Further, because the quad-word of Fossum is addressed with a single address, there is no need for a pointer array, essentially as claimed in Claim 1.

Birrittella teaches multiple overlapped vector memory-reference instructions (see Abstract). Birrittella does not teach or suggest that "entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file" as claimed in Claims 3, 9, 10, 11, 14, 25, and 31, and essentially as claimed in Claims 32-33. Birrittella teaches that a vector unit calculates memory addresses for vector memory-reference instructions (see col. 3, lines 42-45). Similar to Fossum, Birrittella's calculation is not analogous to an addressable word corresponding to a vector, essentially as claimed in Claims 3, 9, 10, 11, 14, 25, and 31-33. For example, see FIG. 2, which illustrates a memory-reference vector instruction. The memory-reference vector instruction includes only a single address of a register and further includes a vector length, implying a contiguous vector, similar to that disclosed by Fossum. Birrittella fails to teach or suggest an addressable word comprising entries have arbitrary addresses, essentially

as claimed in Claims 3, 9, 10, 11, 14, 25, and 31-33. Therefore, Birrittella fails to cure the deficiencies of Fossum.

The combined teachings of Fossum and Birrittella teach a method for calculating addresses of vector memory-reference instructions. The combined teachings of Fossum and Birrittella fails to teach or suggest "entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file" as claimed in Claims 3, 9, 10, 11, 14, 25, and 31-33.

Claims 7, 16-18, 29, and 30 have been rejected under 35 USC 103(a) as being unpatentable over Fossum in view of Birrittella as applied to Claims 3, 14 and 25, and further in view of Sakakibara (USPN 5,392,443). The Examiner stated essentially that the combined teachings of Fossum, Birrittella and Sakakibara teach or suggest all of the limitations of Claims 7, 16-18, 29, and 30.

Claim 7 depends from Claim 3. Claims 16-18 depend from Claim 14. Claims 29 and 30 depend from Claim 25. The dependent claims are believed to be allowable for at least the reasons given for the respective independent claims. Reconsideration of the rejection is respectfully requested.

Claims 5, 6, 27, and 28 have been rejected under 35 USC 103(a) as being unpatentable over Fossum in view of Birrittella as applied to Claims 3, 14 and 25, and further in view of Sakakibara (USPN 5,392,443). The Examiner stated essentially that the combined teachings of Fossum, Birrittella and Sakakibara teach or suggest all of the limitations of Claims 5, 6, 27, and 28.

Claims 5 and 27 are the independent claims.

Claim 5 claims, *inter alia*, "a pointer array electrically coupled by a bus to the vector data file, the pointer array including a plurality of entries wherein each entry identifies at least one storage element in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file, wherein the words are addressed by a word address decoder coupled to the pointer array." Claim 27 claims, *inter alia*, "providing a pointer array having a plurality of entries, wherein each entry identifies at least one storage element in the vector data file for storing at least one data element of the data vectors, wherein for each entry in the pointer array, the at least one storage element identified by the particular entry has an arbitrary starting address in the vector data file, wherein the entries are grouped into addressable words, each addressable word comprising the arbitrary starting addresses corresponding to the storage elements of an individual data vector stored in the vector data file."

As presented above, the combined teachings of Fossum and Birrittella fails to teach or suggest that "entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file."

Sakakibara fails to cure the deficiencies in the combined teachings of Fossum and Birrittella in this regard; Sakakibara teaches that a vector register unit 170 holding actual vector elements (see col. 11, lines 33-40). The vector register unit does not store entries or pointers to a vector data file, essentially as claimed. Indeed, nowhere does Sakakibara teach or suggest the use of a pointer array, much less entries identifying at least one storage element in the vector data file. Therefore, Sakakibara fails to cure the deficiencies in the combined teachings of Fossum and Birrittella.

The combined teachings of Fossum, Birrittella and Sakakibara fail to teach or suggest that "entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file" as claimed in Claims 5 and 27.

Claims 6 and 28 depend from Claims 5 and 27, respectively. The dependent claims are believed to be allowable for at least the reasons given for the respective independent claims. Reconsideration of the rejection is respectfully requested.

For the forgoing reasons, the application, including Claims 3, 5-11, 14, 16-22 and 25, 27-33, is believed to be in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

Respectfully submitted,

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